REMARKS

Claims 1-3 and 5-17 are pending. The title of the invention, the Abstract and claim 10 are amended to obviate minor informalities and not amended to overcome the applied art. No new matter is added. Entry of this Amendment is proper under 35 U.S.C. §1.116 as the amendments merely comply with the requirements set forth in the May 20, 2002 Office Action.

The Office Action objects to the title of the invention due to minor informalities. In particular, the Office Action objects to the term "registered transfer level". By this Amendment, the Title of the Invention is amended to obviate the objection. Accordingly, withdrawal of the objection is respectfully requested.

The Office Action objects to claim 10 due to minor informalities. By this Amendment, claim 10 is amended to obviate the objection. Accordingly, withdrawal of the objection is respectfully requested.

The Office Action rejects claims 1-3 and 5-17 under 35 U.S.C. §102(e) over Dupenloup (U.S. Patent No. 6,296,636). This rejection is respectfully traversed.

Claims 1-3 and 5-9 Define Patentable Subject Matter

In particular, Applicants assert that Dupenloup does not teach or suggest a method of synthesizing a register transfer level based design of a system including at least the steps of determining a plurality of sub-modules of a top level system, determining individual time budgets for each sub-module based on timing requirements of the top-level system, synthesizing gate-level designs of the sub-modules based on the determined time budgets for the individual sub-modules, and testing the gate-level designs for conformance with gate-level design requirements of the individual sub-modules, then integrating the gate-level designs of the

individual sub-modules to form a top level design, as recited in independent claim 1.

Dupenloup discloses a method for generating scripts to synthesize RTL code. See, Abstract, for example. The Dupenloup method uses a complementary approach of top-down characterization and bottom-up synthesis steps. As shown in figure 19, the top-down step is used to provide constraints, time budgets and other information to be met by each module of a larger design. See also, col. 43, lines 16-19, for example. Once the constraints are formed, the various modules are synthesized, then integrated along a design hierarchy. See, col. 41, lines 1-12, for example. Dupenloup does not teach or suggest testing the gate-level designs for conformance with gate-level design requirements of individual sub-modules, then integrating the gate-level designs of the individual sub-modules.

To the contrary, while Dupenloup discloses synthesizing various modules based on time-constraints, nowhere does Dupenloup disclose, suggest or even appreciate any form of individual sub-module testing. See, col. 43, lines 8-26, for example. Although the December 7, 2001 non-final Office Action asserts that Dupenloup discloses "testing the gate-level designs . . . prior to integrating the gate-level designs to form the top-level design (see, page 5, paragraph 7.4 of the Office Action), nowhere do the cited passages disclose or suggest performing any testing whatsoever on individual sub-modules.

While the May 20, 2002 final Office Action claims that Applicants asserted in their March 7, 2002 response that "Dupenloup does not use the word 'test' and therefore Dupenloup cannot anticipate Applicants' limitation", the May 20, 2002 Office Action misconstrues Applicants claim, which was that "nowhere in Dupenloup does the term 'test' **occur in conjunction with individual sub-modules**. Furthermore, neither of Figures 14 or 19 (cited by

the Office Action) show any block or step that suggests any form of **sub-module testing**." {bolded emphasis added}

While the May 20, 2002 Final Office Action further claims that Dupenloup tests gate-level designs for conformance with gate-level design requirements citing col. 30, lines 12-57 and Fig. 1 (see, page 4, second paragraph), the cited passages of the Dupenloup specification do not refer to testing of individual sub-modules. Further, while Fig. 1 does refer to a gate-level verification step **110**, Fig. 1 is an example that demonstrates gate-level verification occurring after a synthesis step **106** is completed and not during synthesis.

Further, a review of Fig. 14, which depicts a three-step process for bottom-up synthesis used by Dupenloup, shows module synthesis and integration, but does not depict any intermediate testing, characterization or verification of sub-modules using gate-level design requirements of individual sub-modules before integration. See also, col. 41, lines 1-12.

Still further, nowhere does Dupenloup show where any gate-level requirements are even generated for individual modules, much less indicate where any testing of gate-level designs for conformance with gate-level design requirements of individual sub-modules is performed. While the Office Action asserts that "determining individual time budgets for each sub-module" is supported by col. 42, lines 29-31, col. 16, lines 6-8, col. 43, line 20 and col. 43, lines 15-18, these passages either merely speak to using time budgets in general and do not even mention sub-modules, or speak to sub-modules without disclosing or suggesting time budgets for submodules. Thus, Dupenloup does not teach or suggest each and every limitation of independent claim 1.

Therefore, independent claim 1 defines patentable subject matter. Claims 2-3 and 5-9 define patentable subject matter by virtue of their dependency as well as for the additional

features they recite. Accordingly, withdrawal of the rejections of claims 1-3 and 5-9 is respectfully requested.

Claims 10-17 Define Patentable Subject Matter

Applicants assert that Dupenloup does not teach or suggest a method of synthesizing an RTL-based design of a system including at least the steps of determining a plurality of sub-modules of a top level system, determining individual time budgets for each sub-module based on timing requirements of the top-level system, . . . generating gate-level netlists for the gate-level designs of each of the sub-modules, and integrating the gate-level designs of the individual sub-modules, as recited in independent claim 10.

Dupenloup does not teach or suggest at least generating gate-level netlists for the gate-level designs of each of a number of sub-modules.

To the contrary, while the Office Action uses the term "netlist" extensively, nowhere does Dupenloup describe generating a netlist from a sub-module. While Dupenloup does state that a "dump script technique used to extract the generic netlist from a Design Compiler has several benefits" (see col. 21, lines 29-33), nowhere does Dupenloup suggest generating a netlist from a sub-module via a "Design Compiler" or otherwise.

Further, while the May 20, 2002 Office Action cites col. 1, lines 34-36 and Fig.1 to support its claim that Dupenloup discloses generating gate-level netlists for the gate-level designs of each of the sub-modules, Applicants point attention to Fig. 1, synthesis step **106**, which merely indicates that some synthesis step occurs. Applicants further point to the cited passage, which states:

> "The IC design, as expressed by the RTL code, is then synthesized to generate a gate-level description, or a netlist[.]"

The above-cited passage clearly does not teach, suggest or even indicate any appreciation for generating gate-level netlists for individual sub-modules.

Furthermore as discussed above, Fig. 14 and its associated text seem to suggest a bottom-up approach where individual modules are created, frozen and then piecemeal integrated entirely within a design compiler, but without generating any intermediate netlists for individual modules. Thus, Dupenloup does not teach or suggest each and every limitation of independent claim 10.

Therefore, independent claim 10 defines patentable subject matter. Claims 11-17 define patentable subject matter by virtue of their dependency as well as for the additional features they recite. Accordingly, withdrawal of the rejections of claims 10-17 is respectfully requested.

CONCLUSION

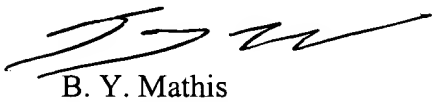
Applicants believe that this application is in condition for allowance and Applicants request that the Examiner give the application favorable consideration and permit it to issue as a patent. However, if the Examiner believes that the Application can be put in even better condition for allowance, the Examiner is invited to contact Applicants' representative listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including

extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



B. Y. Mathis
Registration No. 44,907

600 13th Street, N.W.
Washington, D.C. 20005
(202) 756-8000 BYM/JAH:kap
Facsimile: (202) 756-8087
Date: July 22, 2002

Attachments:
Appendix With Markings to Show Changes Made

APPENDIX WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE:

The title has been amended as follows: "BOTTOM-UP APPROACH FOR SYNTHESIS OF [REGISTERED] REGISTER TRANSFER LEVEL (RTL) BASED DESIGN"

IN THE CLAIMS:

Claim 10 has been amended as follows:

10. (Amended) A method of synthesizing a register transfer level (RTL) based design of a system comprising the steps of:

determining [sub-module] sub-modules of a top level system;

determining individual time budgets for each sub-module based on timing requirements of the top-level system

synthesizing gate-level designs of the sub-module based on the determined time budgets for the individual sub-modules;

integrating the gate-level designs of the individual sub-modules to form a top level design;

testing the top-level design for conformance with top-level design requirements;

generating gate-level netlists for the gate-level designs of each of the sub-modules; and

generating a top-level netlist when the top-level design conforms to the top-level design requirements.

IN THE ABSTRACT:

The Abstract has been amended as follows:

ABSTRACT

A method for synthesizing a [registered] register transfer level (RTL) based design employs a bottom-up approach to generate a final top-level design. The top-level design is divided into a plurality of sub-modules. Each of the sub-modules is then independently synthesized using an RTL based design approach and independently adapted to conform to timing requirements produced for each of the sub-modules using time budgets that are based on the top-level timing requirements. Once the sub-modules are synthesized and pass individual timing requirements specific for those sub-modules, the sub-modules are integrated to form a top-level design. The top-level design may then be verified for timing requirements and other formal requirements.